Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques

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***Abstract*—A new concept for packaging high frequency monolithic circuits is presented. It consists of developing miniaturized housings to shield individual passive components (e.g., CPW based), active elements, or combinations of them by employing silicon micromachining technology. At high frequencies, self-packaged configurations that are fabricated in this manner provide reduction in the overall size and weight of a circuit and provide increased isolation between neighboring circuits. Therefore, the resulting characteristics make these micropackaged components appropriate for high density, multilevel interconnect circuits. This paper will describe the fabrication procedures used to develop self-packaged components. Performance curves for typical high frequency circuit geometries that are implemented in this configuration are shown for measured and theoretical results.**

I. Introduction

MICROWAVE and millimeter wave circuit design relies heavily on the use of planar transmission lines such as microstrip, stripline, slotline, and coplanar waveguide to achieve design flexibility as well as ease in mounting active components. While inherit advantages are offered within each of the existing technologies, limitations are still present and are related primarily to issues regarding parasitic mechanisms such as electromagnetic coupling and parasitic radiation. Since circuit performance is often time compromised and successful designs are conditional on circuit performance requirements, the development of a novel circuit geometry that offers the capability to minimize these effects is warranted. One solution, therefore, is to provide shielding to individual circuit components while preserving the structural characteristics of the conventional uniplanar technology. This approach can provide a new dimension to high frequency circuit design and can allow for more compact circuit configurations which consequently address the issue of high density packaging. These individually shielded circuit components are achieved by developing monolithic cavities, referred to as "micropackages," around existing planar circuits through novel use of well established Si or GaAs micromachining technologies. This results in improved circuit performance due to the reduction of parasitic electromagnetic coupling in the substrate (substrate modes) and air (space waves).

In typical applications, where metallic housings are used to protect circuit components from the environment, unwanted parasitics, and multiple resonances are introduced due to the presence of a large metallic shielding package. Micropackaging, on the other hand, eliminates those resonances by developing shielded structures that are small in size, can follow individual circuit paths, and can be fabricated monolithically with the circuit. Additionally, micropackages are also easily compatible and integratable with existing conventional circuit arrangements and can be designed to electrically and/or hermetically encapsulate planar circuit components or subsystems. These self-packaged circuits can therefore be effectively used within larger conventional housing structures either hybridly using a flip-chip technology or monolithically in a miniaturized package configuration where the circuit response is now electrically decoupled from interactions with the larger metallic package.

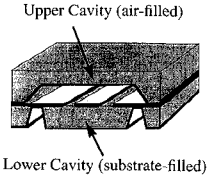

Fig. 1. Three-dimensional cross section of a micropackaged circuit where the shield and line are integrated monolithically.

RF micromachining, while still in its infancy, has been recently used in the development of monolithic waveguides [1] and high performance membrane-supported circuits [2]. Even though micromachining of silicon is a well-established technology for sensor and biomedical applications, many other applications exist in high frequency circuit design that can benefit from its use. In an effort to outline the potential of this technology, this article addresses packaging issues and presents the development of the first generation of micromachined, self-packaged circuits. The circuit components presented are primarily of coplanar waveguide (CPW) type and are surrounded by an air-filled cavity in the upper region and a substrate-filled cavity in the lower region as shown in Fig. 1. Since comprehensive understanding of fabrication capabilities is critical for the development of these circuits, an extensive study of various fabrication techniques has been performed and a brief description of the findings is presented. While the structures presented in this paper represent only one approach for implementing micromachining techniques to high frequency applications, several basic elements have been chosen to illustrate the applicability of this technology in this area. These simple components consist of tuning stubs and filters that are developed, measured and compared to the

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performance of theoretical results. In Section II-A, a general overview of the design approach is given followed by an extensive discussion of the fabrication procedures developed and implemented. In Section II-B, measurement considerations are discussed, fundamental line characteristics are presented, and experimental results for various circuit components such as tuning stub elements and filters are shown.

II. Development of Micromachined Circuits

To illustrate the versatility of micromachining, this effort concentrates on developing circuits that reside in partially or completely shielded environments. Poor electrical performance of circuits operating in open environments is attributed to free-space radiation and substrate mode excitation, while in shielded environments it is mainly due to package resonances. The open environment described herein refers to circuits which are printed on a dielectric substrate and radiate into free space. On the other hand, the term "shielded geometries" implies circuits which are partially or completely shielded by cavities in the upper and/or lower regions. Since substrate modes occur in the dielectric substrate, the introduction of physical alterations to the substrate itself can result in elimination of these parasitic waves and in improvement of circuit performance. The following sections outline the steps needed to design the circuits mentioned above and extensively describe the silicon (Si) fabrication processes required for their development.

A. Design Approach

The first step in the design of high-frequency circuits is the specification of the geometrical parameters needed to provide the desired electrical response. While there exists a wide variety of commercially available computer-aided design (CAD) tools for low-frequency applications, software for high-frequency design is currently unavailable. Despite the lack of CAD software at these frequencies, there are a number of circuit simulations tools that can be used indirectly in design to produce satisfactory analysis results, even though, very long design cycles, and extensive computation times are typically required. The micromachined self-packaged circuits presented here have been designed through such an iterative approach. In this scheme, first low-frequency software models that use quasi-static approximations [3], [4] provide the initial design, then the geometrical parameters are modified in an iterative manner and realized. Lastly the circuit performance is predicted using the high-frequency analysis software which is based on full-wave models in frequency or time domains [5]–[12]. When the predicted electrical response closely matches the desired one, this iterative cycle is terminated.

Concurrently the issue of package resonances and substrate mode excitation are also addressed. As it has been extensively described in the literature [13], [14], electrical packages can greatly affect circuit performance either through package resonances or through proximity coupling. The first effect is mostly related to the dimensions of the package while the latter is due to cross-coupling of neighboring circuits. Unfortunately these two mechanisms require contradicting approaches which lead to design trade-offs. Ideally, a given circuit has an optimum package size that is small enough to eliminate resonances within the range of operating frequencies and that is physically far enough away from the circuitry so that it does not interfere with the circuit's electrical performance. Although circuits in open environments do not face the previously described problems, they are prone to parasitic radiation which is mostly associated with the excitation of substrate modes. Since the excitation of these modes is mostly dependent on the operating frequency and the physical thickness of the substrate, careful layout configurations in less dense circuit environments can sometimes reduce such parasitic radiation, provided there is flexibility in circuit placement. In practical applications, however, circuit requirements greatly limit the flexibility in rearranging the location of the various circuit components such that any layout modifications, at least, can only weakly reduce such parasitic loss [15].

During the characterization efforts performed, preliminary findings indicate that substrate modifications alone may have a substantial impact on substrate mode excitation. While researchers have been aware of the issues discussed above in planar designs since the late seventies, the existing technology at that time could not provide alternative solutions to reduce the substrate mode excitation. Recent advances in silicon micromachining techniques, however, allow for unique, yet simple practical solutions to the above problems. In the development of micropackages, dimensions can be chosen simply by using waveguide and cavity models to predict geometrical dimensions that avoid unwanted resonances. In addition, the shape of the cavity can be designed so that it follows the circuit and does not physically affect its performance. For open circuits, substrate modifications using micromachining can be implemented to eliminate these unwanted substrate modes entirely, resulting in improved circuit performance.

B. Fabrication Procedures

The micromachined circuits described herein are comprised of a two-silicon (Si) wafer system having a $\langle 100 \rangle$ orientation and primarily utilize silicon micromachining processes, which are fairly standard in sensor applications but are relatively new to high frequency circuit design. This section presents an extensive discussion on the fabrication steps required for the development of self-packaged circuits and provides a detailed description of the employed processes.

All circuits presented are of coplanar type, printed on Si, and shielded by miniature cavities in both or either of the upper and lower surrounding regions. As seen in Fig. 1, the upper region consists of a metallized air-filled cavity while the lower region is a substrate-filled cavity that is metallized on the lower side. Since the circuits are printed on the lower wafer, high resistivity silicon with $\epsilon_r = 11.7$ is required. In this configuration the upper and lower cavity regions provide ground plane equalization through direct contact with the ground planes of the coplanar waveguide lines. Important issues to consider during design include the fabrication of accurate alignment marks between the various wafers, the design of appropriate feeding lines for individual circuit exci-

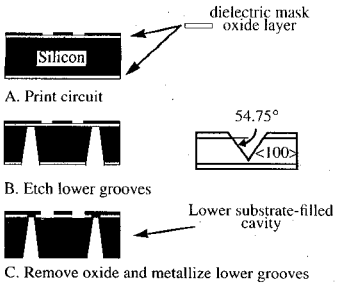

Fig. 2. Lower wafer development. (a) Transmission lines are printed on the top surface. (b) Lower cavity is formed by etching v-grooves. (c) Lower cavity grooves are metallized below the line forming direct contact to the upper ground planes.

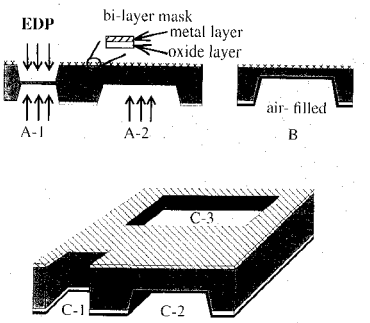

Fig. 3. Upper wafer development. (a) Probe windows and alignment marks (A-1) are etched from both sides while the upper cavity (A-2) is etched from one side only. (b) The upper cavity is then metallized. (c) Finally, the upper wafer sectional view after processing with the alignment marks (C-1), upper cavity (C-2) and the probe window (C-3).

tation, and the development of enclosing environments that can be integrated monolithically with the specific circuits without degrading the electrical performance. The following sections address these concerns comprehensively while describing the technique used for individual wafer development.

The lower wafer scheme shown in Fig. 2 is a high resistivity, single-side polished, 350 micron thick silicon substrate having a silicon dioxide dielectric layer that has been thermally grown to 1.2 micron thickness. Since this wafer contains the planar lines and lower cavity region of the circuit, oxide regions are removed on the upper surface using buffered hydrofluoric acid (BHF) to allow ground plane equalization of the lower shield to coplanar waveguide ground plane. The planar circuits are then defined using standard photolithographic techniques and electroplated to achieve a three micron metal thickness after evaporating a seed layer of titanium/gold/titanium (Ti/Al/Ti). Once the circuits and alignment marks have been printed, the backside of the wafer is patterned photolithographically to define the lower cavity regions using an infrared (IR) alignment procedure. Prior to anisotropically etching the silicon, the oxide is removed from these regions that define the cavity sidewalls using buffered hydrofluoric acid (BHF). The anisotropic etchant, ethylene diamine pyrocatechol (EDP), uses the $\langle 111 \rangle$ crystal plane as an etch stop for $\langle 100 \rangle$ silicon wafers and results in an etch angle profile of 54.75° [16]. The cavity formation has pyramidal sidewalls as seen in Fig. 2(b), where the lower cavity is the substrate-filled one shown with its widest dimension at the upper surface and narrowest dimension at the bottom of the cavity [Fig. 2(c)], simulating an inverted pyramid. The lower cavity shielding formation is complete after a seed layer of Ti/Au is evaporated and electroplated on the backside of the wafer to three microns.

The upper wafer scheme, shown in Fig. 3, contains both upper cavities and alignment marks that are formed by etching from both sides of the wafer. Since these cavities provide ground plane equalization and shielding without interfering with the signal path, it is not necessary to use high resistivity Si. The upper shielding in this work is developed using a 500 micron thick low resistivity Si with 7500 Å of thermally grown oxide. After defining the probe window and alignment marks using photolithogrpahy, a metal lift-off procedure is employed to open the areas to be etched and to provide an additional masking layer of Ti/Au metal on the backside of the wafer. This layer serves two purposes: it offers protection on the back of the cavity regions and it acts as a mask during backside IR alignment. On the lower side, the cavities are defined and the oxide is removed to expose the silicon surface as shown in Fig. 3. The patterns are then etched in EDP to a desired dimension that is monitored using "etch rulers," which consist of rectangular widths corresponding to specific etch depths. Since this wafer must be handled frequently after etching the multiple cavities and windows, additional mechanical strength can be provided by including a structural beam, located in the middle of the probe window, as seen in Fig. 4.

After fabrication, the upper cavities are aligned to the planar circuits with lower cavities that are located on the upper and lower wafers, respectively. The two wafers are then bonded together to complete the formation of the micropackage (Fig. 5). While the above procedures concentrate on the development of a completely shielded or self-packaged configuration, partially shielded structures can also be obtained by implementing procedures presented in either the upper or lower wafer development scheme.

III. Experimental Characterization of Partially and Completely Shielded Circuits

A. Measurement Considerations

To measure circuit performance up to 40 GHz, conventional on-wafer characterization is utilized in conjunction with the thru-reflect-line (TRL) calibration technique [17]–[19]. The measurement set-up consists of an HP 8510B Network Analyzer that operates up to 40 GHz, an Alessi probe station, and Cascade Microtech ground-signal-ground (GSG) probes that have a probe pitch[1] of 150 μm. This calibration is achieved using standards that include upper and lower shielded regions that are identical to those of the circuits of interest and that are developed using the fabrication procedures described previously. A one tier de-embedding technique is used for on-wafer probing which calibrates the system reference plane to a point within the shielded transmission line. This results in characterization of all transitions located between the input and output ports of the ANA and the newly defined reference plane.

[1] Pitch is defined as the separation between the signal line and the ground plane of the coplanar GSG probes.

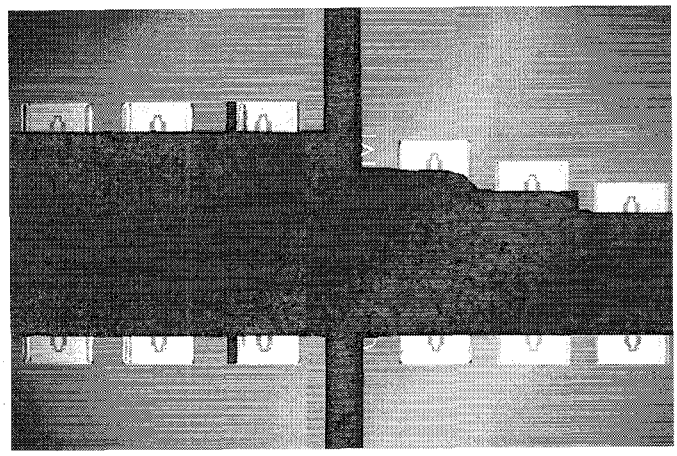

Fig. 4. Photograph of completely shielded circuit from the top view where the probe windows the open areas and are shown in relation to the circuit printed on the lower wafer. The dark vertical bar represents the support beam of the upper wafer.

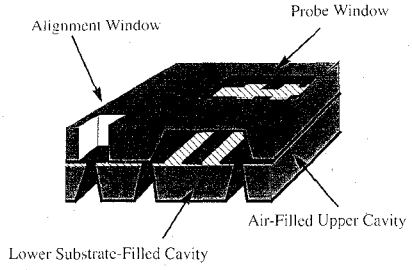

Fig. 5. Completely shielded micropackaged circuit with lower and upper wafer alignment.

Measurements have been performed on partially and completely shielded configurations and are completed in two steps. Circuits with upper shielding only, are characterized first. In this arrangement, the cavities are mounted on the coplanar waveguide (CPW) circuits and the whole structure is placed on a duroid substrate with ϵ_r =2.2 and thickness of 3.175 mm in order to prevent the formation of a parallel plate waveguide between the ground planes of the CPW and the wafer chuck. The next step of this investigation deals with the characterization of various circuit geometries which are completely shielded as it has been described in the previous section. Since the circuits under test are completely isolated from the outside environment, they are placed directly onto the probe station wafer chuck in the measurement set-up.

The characterization of partially as well as entirely self-packaged circuits can provide a very comprehensive understanding of the effect of micropackaging on circuit performance. The following sections present a systematic theoretical and experimental investigation which has been performed on a variety of circuits. These circuits can be grouped into three categories: (a) circuits with upper shielding (US), (b) circuits with lower shielding (LS), and (c) circuits with complete shielding (CS).

B. Delay Lines and Cavity Dimensions

To accurately characterize the presented micromachined geometries, the first issue to address is the development of feeding lines to provide the appropriate excitation. Since the measurement system reference impedance is 50 ohms, the feedline dimensions are determined to meet this requirement. For the circuit components presented in this paper, the feedlines are designed using CAD tools available at the University of Michigan [3]. For the on-wafer probe station, coplanar waveguide feedlines are designed to have a 100 micron center conductor width and a 60 micron slot width, which were determined using design equations from Ghione *et al.* [20]. For matching 50 ohm impedances in the shielded region, the planar line dimensions are 180 and 130 microns for the center conductor and slot widths, respectively. The cavity dimensions used in this case are shown in Table I of Fig. 6.

TABLE I
CROSS SECTIONAL DIMENSIONS OF SHIELDED CIRCUITS

Cavity	height	width-max	width -min
Upper	280	1200	800
Lower	350	950	500

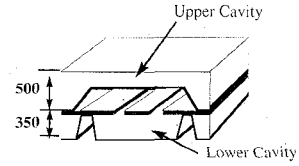

Fig. 6. Dimensions for the completely shielded micropackaged circuit in microns.

The micromachined circuits in this study can have several transitions to minimize the mismatch between the probe and shielded geometries (Fig. 7). Specifically, completely shielded and partially shielded structure have similar transitions, although in one case, half of the shielded region is absent. The first transition occurs between two 50 ohm sections of grounded CPW (GCPW) where the first section (A-B) is the probe feeding pad which has a center conductor width of 100 microns and a slot width of 60 microns. This tapers outward to a wider line (B-C) having a center conductor width and slot width of 180 and 130 microns, respectively. The next transition is a discontinuity at the D-D′ plane that occurs between the open GCPW line and the completely shielded GCPW. At this transition the conducting line dimensions remain the same, but an upper shield has been integrated monolithically and has dimensions that are chosen such that the impedance of the line is not effected by the presence of the shield. The lower cavity width is the minimum required to avoid sidewall interference with the field confinement in the slots. Since the calibration reference planes are located in side this shielded region, all measured circuits have similar feedline transitions to allow use of the same calibration standard set.

The response of a through line for open CPW and upper shielded (US) CPW has been measured and results are shown on Fig. 8. As indicated by these results, the open CPW line suffers from parasitic radiation in the form of substrate modes which is indicated by the ripple shown in the data toward the higher frequency end of the band. When the same line is packaged in the upper air region only, coupling into substrate modes is reduced resulting in a flatter response over the entire frequency range.

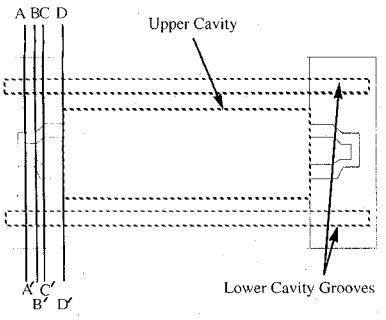

Fig. 7. Various transitions of a completely shielded micropackaged circuit used for on-wafer probing calibration.

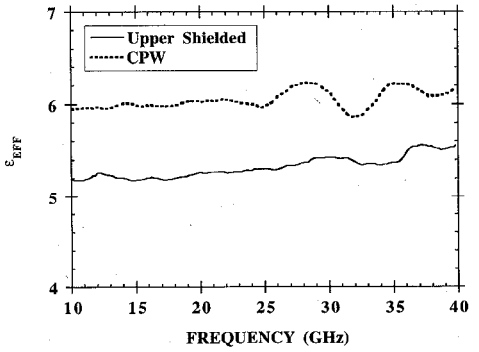

Fig. 8. Effective dielectric constant for an upper shielded (US) and open CPW through line.

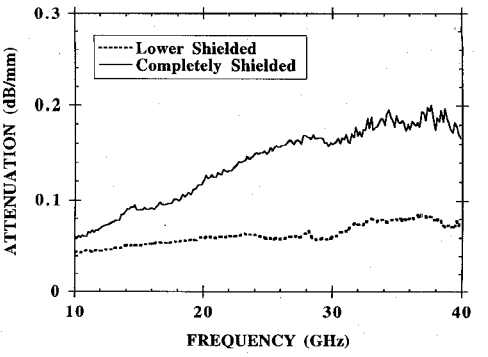

Fig. 9. Attenuation constant for a completely shielded (CS) and lower shielded (LS) through line.

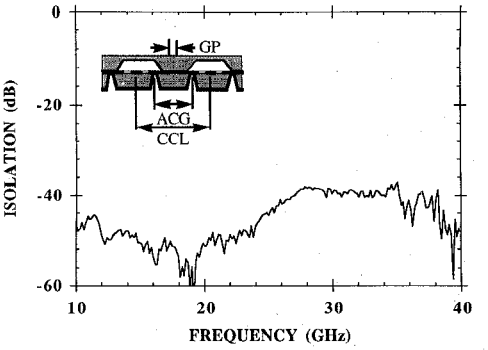

Fig. 10. Isolation response between two completely shielded delay lines, where delay lines 1 and 2 are 3732 and 3242 microns, respectively. These lines have adjacent ground planes (GP), adjacent channel grooves (ACG) and center conducting lines (CCL) separated by 836, 1330, and 2546 microns, respectively.

For the lower shielded (LS) and completely shielded (CS) through line, a plot is shown in Fig. 9 for the line attenuation in dB/mm which includes the effects of both dielectric and conductor loss. The results indicate that the lower shielded line has performance comparable to data presented by Taub [21] for losses in coplanar waveguide which is printed on silicon wafers with similar resistivity (3000 ohm-cm) and with the same aspect ratios. It is interesting to observe that attenuation in the completely shielded line (CS) is slightly higher than the lower shielded line (LS) due to additional conductor loss that is present in the upper shield. In conclusion, the data shown indicate that both LS and CS cases provide a favorable alternative to the use of grounded CPW which is known to suffer from excitation of substrate modes. In the open-end series stub section discussed later, a more thorough description of micropackaging effects on circuit performance will be presented to show the benefits of either partial or complete shielding compared to open environment circuit designs.

For circuit isolation of a completely shielded configuration, two delays lines, whose length differ by 510 microns, are measured where the input signal goes into port 1 of the shorter line and the output signal is measured from port 2 of the longer delay line. The resulting measured isolation is at least −40 dB across the band as seen in Fig. 10 for circuits that are separated by approximately 2.54 mm.

C. Short-End Tuning Stub

Various simple discontinuities are implemented to show the realization of conventional circuits into micromachined self-packaged design configurations. Fig. 11 shows the physical dimensions of a series short-end tuning stub element [22] located within a completely shielded embodiment while Fig. 12 shows a comparison between measured and full wave analysis results. The theoretical and experimental data are plotted and show similar electrical performance except for a shift in the resonant frequency which is attributed to the geometrical variations between the model and actual circuit geometry. Since the theoretical results do not account for losses, the difference in the level of the transmission coefficients is expected. Another geometrical variation that may also be responsible for the observed differences is the trapezoidal shape of the cavity walls as opposed to the rectangular shape assumed by the models. These effects can alter the circuit parasitic capacitances, thus, modifying the bandwidth and resonant frequency. Lastly, since the model assumes perfectly rectangular corners in the stub fingers, the measured line lengths can appear electrically shorter since the stub fingers suffer from rounding of corners and edges as a result of the fabrication procedures.

D. Filters

A five-section stepped-impedance CS lowpass filter has been designed as shown in Fig. 13 with high and low impedances of 100 Ω and 20 Ω, respectively. Figs. 14 and 15 show a comparison between measurements and theoretical results derived from quasi-static models with both conductor and dielectric losses are accounted. In the PUFF [4] model, care

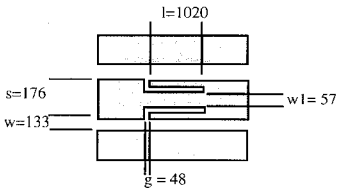

Fig. 11. Series short-end tuning stub dimensions in microns.

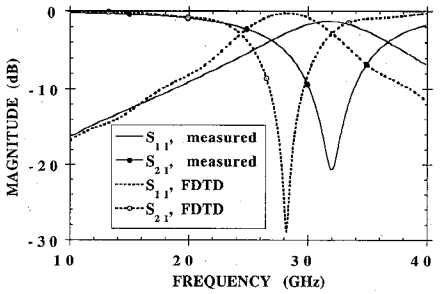

Fig. 12. Comparison between FDTD model and measured results for reflection ($S11$) and transmission ($S21$) coefficients of a completely shielded short-end tuning stub.

was taken to incorporate the specific metallization thickness and the appropriate surface resistivity which correspond to the various sections of microstrip line widths. To realize 100 and 20 ohm impedance steps, 20 and 380 micron wide conductor lines are used with slot widths of 210 and 30 microns. In the low impedance section, the line excites a coplanar waveguide mode due to the narrow slot width while the high impedance section excites a microstrip mode. This mixed-mode operation produces parasitic inductances and capacitances that cannot be easily accounted for in the quasi-static model. Despite this limitation however, at relatively low operating frequencies the effects of such parasitics are reduced and, as seen in Figs. 14 and 15, the measurements agree very well with the theoretical data. The total system loss, $(1 - |S_{11}|^2 - |S_{21}|^2)$, shown in Fig. 16 shows good agreement between theory and measured results. This indicates that the circuit has negligible radiation loss and thereby confirms the effectiveness of the micropackage. The level of loss can be attributed to the aspect ratios of the low and high impedance sections which are known to cause higher loss in both the coplanar waveguide mode [23] and the microstrip mode [24]. Additional validation of the response of a self-packaged filter, shown in Fig. 17, is provided through a comparison between a theoretical model based on finite difference time domain (FDTD) and experimental measurements. Even though loss effects have been neglected in the model, excellent agreement is observed between the results.

E. Open End Tuning Stube

The open-ended tuning stub [22] shown in Fig. 18 will be used to illustrate the electromagnetic effects from a variety of micropackaging configurations. Performance curves will be shown for the upper (US), lower (LS), and completely shielded (CS) configurations. These results will be compared to open CPW and a discussion will be presented on the nature of the various effects on the circuit response.

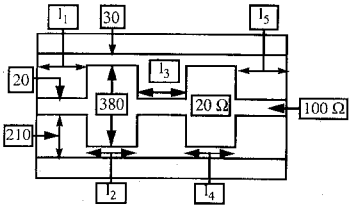

Fig. 13. Dimensions of a five-section stepped impedance lowpass filter having low impedance sections of 20 ohms and high impedance sections of 100 ohms.

TABLE II
ACTUAL CIRCUIT DIMENSIONS

Line Lengths (microns)
l_1= 988
l_2=703
l_3=940
l_4=722
l_5=988

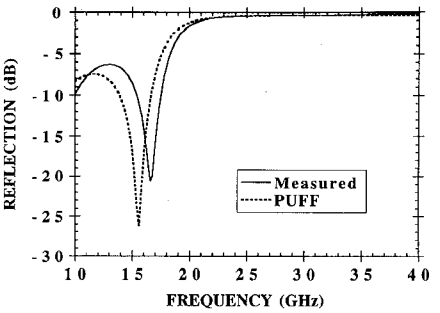

Fig. 14. Comparison of reflection coefficient between the PUFF model and measured results for a five-section stepped impedance lowpass filter.

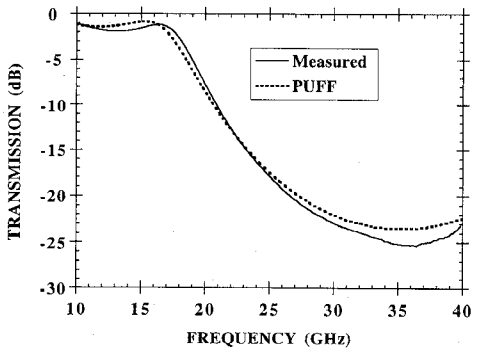

Fig. 15. Comparison of transmission coefficient between the PUFF model and measured results for a five-section stepped impedance lowpass filter.

In the case of open CPW, loosely bound fields tend to leak power strongly and destructively into substrate modes. When shielding occurs in either or both regions, the propagating modes become tightly bound to the line and radiation is reduced significantly compared to the case of the open CPW. The circuit performance shown in Fig. 19 compares the open CPW to the CS geometry. The open CPW shows performance degradation above 25 GHz due to the excitation of a strong substrate mode, while completely shielded circuits exhibit a very smooth response even at higher frequencies due to reduction of parasitic radiation and surface waves. When comparing the US to the LS configuration (Fig. 20) for the

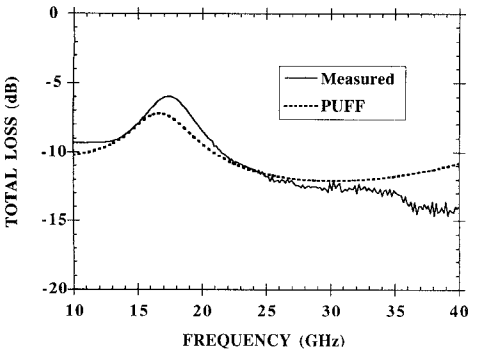

Fig. 16. Loss comparison between the PUFF model and measured response for a five-section stepped impedance lowpass filter.

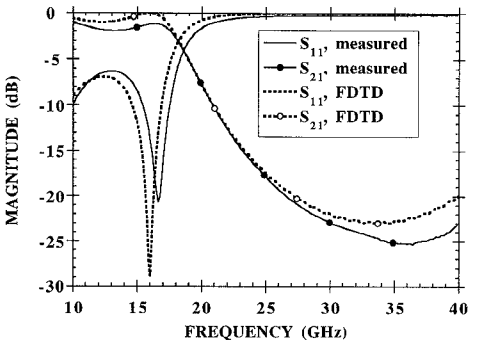

Fig. 17. Comparison between the FDTD model and measured results for reflection ($S11$) and transmission ($S21$) coefficients of a five-section stepped impedance lowpass filter.

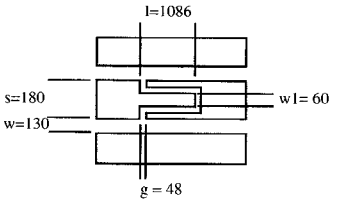

Fig. 18. Series open-end tuning stub circuit dimensions in microns.

same circuit geometry, the LS has the smoothest response due to the substantial reduction of substrate leakage. Although the circuit performance for the US show a few ripples at the higher frequencies, overall performance improvements are observed as a nearly symmetric response is obtained. While the LS and CS scattering parameter measurments appear virtually identical in Figs. 19 and 20, existing differences will become more apparent when observing the total loss data.

A comparison between the total loss of self-packaged components and open environment components, as seen in Fig. 21, shows that open configurations exhibit the highest overall loss. Of the self-packaged components, the US configuration has the highest loss which is mainly due to conductor loss and excitation of a strong surface waves. The lowest loss is presented by the LS geometry since the fields are primarily confined in the dielectric-filled cavity causing a reduction of parasitic radiation effects into air. In these circuits the LS package size is chosen to be small enough to suppress unwanted resonances. Lastly, the CS geometry exhibits loss performance that is compromised slightly when compared to

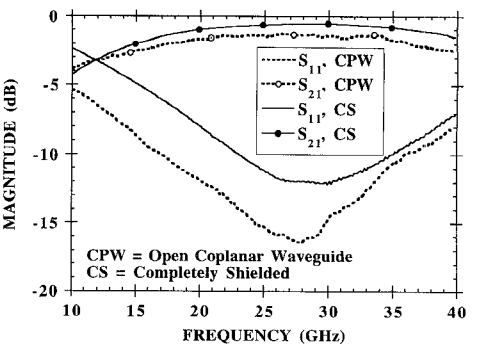

Fig. 19. Comparison of reflection ($S11$) and transmission ($S21$) coefficients between open and completely shielded CPW environments of an open-end series stub.

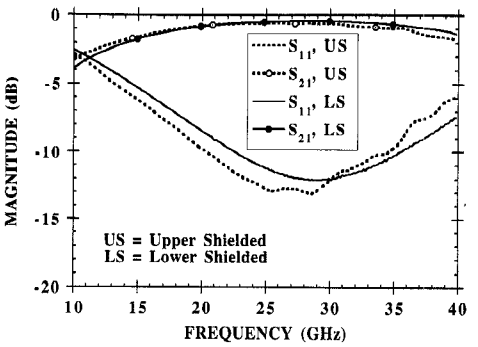

Fig 20. Comparison of reflection ($S11$) and transmission ($S21$) coefficients between upper and lower shielded CPW environments for an open-end series stub.

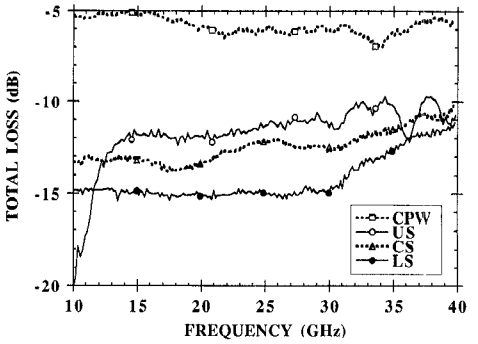

Fig. 21. Loss comparison of an open-end series stub in open (CPW), upper (US), lower (LS), and completely shielded (CS) environments.

the LS case due to the presence of the upper shield. In general, however, micropackages with partially or completely shielded environments can offer significant improvement in electrical performance over open environment circuits. In instances where maximum reduction in loss is needed, the lower shielded configuration is the ideal choice while optimum isolation in either or both regions requires use of the completely shielded configuration.

IV. Conclusion

The development of micromachined cavities for micropackaging of high frequency circuits has been proven successful. The fabrication of these structures has been presented and

measured data have been compared to theoretical results. The response of simple circuit geometries used in conventional planar line designs were implemented as through lines, series tuning stubs, and a stepped impedance lowpass filter. Since the derived data show that the monolithic incorporation of a shielding cavity with the circuit results in improved performance, "self-packaged" configurations provide the ability to evaluate specific designs more comprehensively. Lastly, as a result of the good agreement between measured data and theoretical predictions for basic components, the above study strongly indicates the potential of micropackaged circuits in high frequency circuit applications.

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